
ANAGRAM Hardware for HiFi™ Family
TimeLock™ Ultra-Low Jitter Clock
Module Data Sheet
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Abstract

TimeLock™ ultra-low jitter master clock generator.

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Part Number	Description
TLM-PB-110A	ANAGRAM TimeLock Product Brief.
TLE-UM-110A	ANAGRAM TimeLock Evaluation Board User Manual.

Ordering Information

Part Number	Description	Package
TLM-PL-110A	ANAGRAM TimeLock ultra-low jitter master clock generator 24.5760MHz	Plastic

Release Notice

This document is under configuration control and updates will only be issued as a replacement document with a new version number.

Preface

About This Data Sheet

This document provides the information needed to design and integrate the TimeLock™ precision master clock generator module into your product. For more information about this product, please refer to the product description available from the ANAGRAM Technologies web site at <http://www.anagramtech.com>.

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It is important to operate this product within the specified input and output ranges described in the Data Sheet. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the Module. If there are questions concerning the input range, please contact ANAGRAM Technologies customer support prior to connecting the input power. Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the Module. Please consult the Data

Sheet prior to connecting any load to the Module. If there is uncertainty as to the load specification, please contact ANAGRAM Technologies customer support.

How to Use This Document

Throughout this document, the abbreviation TLM and the term *TimeLock™ Module* are synonymous with the TimeLock™ precision master clock generator.


Chapter 1 Overview of the TimeLock™ Module functionality.


Chapter 2 Electrical and performance characteristics.

Chapter 3 Interfacing and application information for hardware and system engineers.

Chapter 4 Mechanical and packaging information.

Information About Cautions and Warnings

Note	
	<p>A NOTE provides additional or special information to assist operation and maintenance personnel. Disregarding a NOTE may cause inconvenience but will not result in personal injury or equipment damage.</p>

Caution	
	<p>A CAUTION is provided in a procedure whenever electrical or mechanical damage may occur. Failure to heed a CAUTION may result in some form of damage to the equipment; however, personal injury is unlikely.</p>

If You Need Assistance

If you have questions regarding either the use of this module or the information contained in the accompanying documentation, please contact the ANAGRAM Technologies Customer Support +41 (21) 804-1960 or visit the ANAGRAM Technologies web site at <http://www.anagramtech.com>.

Repair and Maintenance

Routine maintenance is not required. This product named as TimeLock™ Module is warranted to be free of any defect with respect to performance, quality, reliability and workmanship for a period of SIX (6) months from the date of shipment from ANAGRAM Technologies SA.

In the event that your product proves to be defective in any way during this warranty period, we will gladly repair or replace this piece of equipment with a unit of equal or superior performance characteristics.

Should you find this TimeLock™ Module has failed after your warranty period has expired, we will repair your defective piece of equipment for as long as suitable replacement components are available. You, the owner, will bear any labor and/or component costs incurred in the repair or refurbishment of said equipment, beyond the SIX (6) months warranty period. Any attempt to repair this product by anyone during this period other than by ANAGRAM Technologies SA or any authorized 3rd party, will void your warranty.

ANAGRAM Technologies SA reserves the right to assess any modifications or repairs made by you and decide if they fall within warranty limitations, should you decide to return your product for repair. In no event shall ANAGRAM Technologies SA be liable for direct, indirect, special, incidental, or consequential damages (including loss and profits) incurred by the use of this product. Implied warranties are expressly limited to the duration of this warranty.

A Return Material Authorization number (RMA) will be issued to you, as well, as specific shipping instructions, should you wish our factory to repair your TimeLock™ Module. The RMA number has to be requested from ANAGRAM Technologies S.A before sending back the failed module.

A temporary replacement, if required, will be made available for a nominal charge. Any shipping costs incurred, will be the responsibility of the customer. All products shipped to you from ANAGRAM Technologies SA, will be shipped collect.

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1 Introduction

This chapter gives a brief introduction to the features and principle technologies behind the TimeLock™ Module, a high precision, ultra-low jitter clock generator.



Figure 1: Photo of TimeLock™ module.

1.1 Highlights

The TimeLock™ Module is an ultra-low jitter master clock generator for high end, pro and consumer audio applications. Key features for the TimeLock™ Module include:

- Superior jitter performance (<1ps RMS phase jitter @ 25MHz).
- Outputs able to drive 12 series terminated lines.
- 3 LVCMOS/LVTTL outputs.
- Incorporates high quality pure quartz crystal.
- Synchronous output clock enables.
- High quality separate linear regulators for clock generator circuitry.

1.2 Functional Block Diagram

The TimeLock™ Module integrates high quality linear regulation and an ultra-low jitter master clock generation circuitry that allows a super clean, stable clock to drive critical IC components in demanding audio applications. The module features a single control input, clock enable, a digital power supply input, and three clock outputs. The main clock output has a series resistance of 50Ω configured to directly drive one-to-one series terminated LVCMOS receivers. Two auxiliary clock outputs that allow flexible clock line terminations.

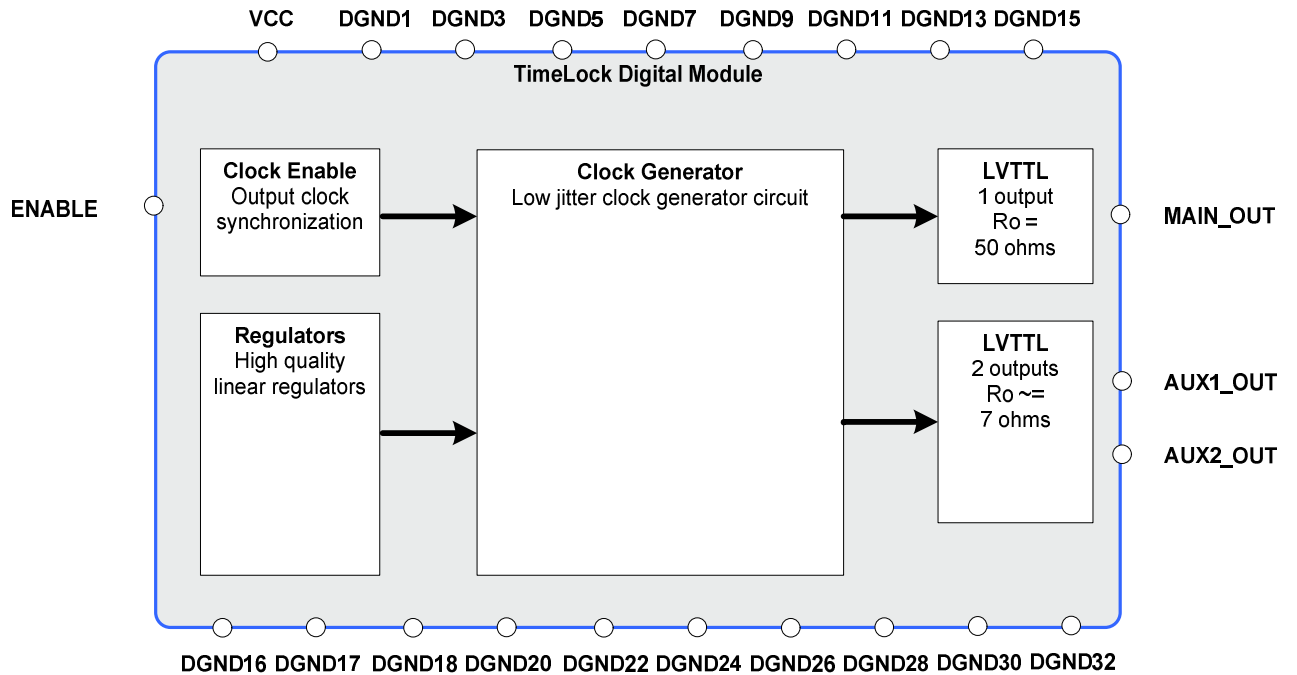


Figure 2: Functional block diagram.

1.3 DSS™ Clock Synchronization

The TimeLock™ Module is a high quality clock source for system that employ a concept of clock management called DSS™ synchronization which allows the system to handle a variety of sampling rates and data formats. DSS™ provides an elegant, cost effective, and future proof solution by synchronizing the complete audio system to a reference clock source (TimeLock™) and unifying data to a single sampling rate as show in Figure 3.

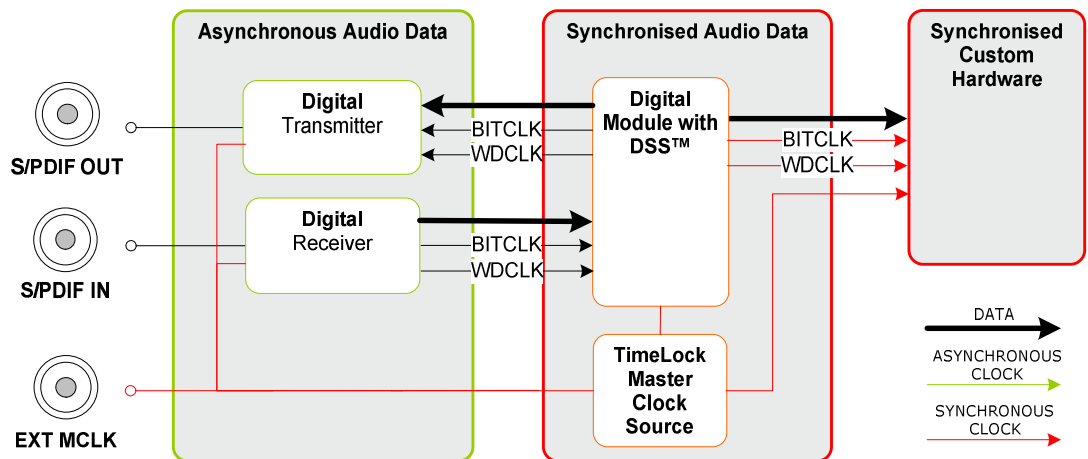



Figure 3: Clock domain block diagram illustrating DSS™ Clock Synchronization.

2 Characteristics and Specifications

This chapter identifies important information regarding the TimeLock™ Module that you should know before getting started.

2.1 Electrostatic Discharge Warning

Many of the components in the TimeLock™ Module are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the TimeLock™ Module, including the use of a grounded wrist strap at an approved ESD workstation.

Caution	
	<i>Failure to observe ESD handling procedures may result in damage to the TimeLock Module.</i>

2.2 Recommended Operating Conditions

Hereafter is given recommended conditions where the module should work properly. Exceeding these conditions is not advisable but acceptable. Table 1 summarizes the recommended data points.

Parameter	Recommended Condition	
Power Supply	$V_{CC(\min)}$: +4.7V	
Clock Enable	$V_{IL(\min/\max)}$: -0.3V / +0.8V	$V_{IH(\min/\max)}$: +2.0 / +3.6V


Table 1: Recommended operating ratings.

2.3 Absolute Maximum Operating Conditions

The user should be aware of the absolute maximum operating conditions for the TimeLock™ Module. Exceeding these conditions may result in damage to the TLM. Table 2 summarizes the critical data points.

Parameter	Maximum Condition
Power Supply	-30V / +30V
Clock Enable	-20V / +20V

Table 2: Absolute maximum ratings.

Caution	
	<i>Failure to respect the Absolute Maximum Operating conditions may result in damage to the internal TimeLock™ Module components.</i>

2.4 Performance Specifications

Parameter	Min	Typ	Max	Units
Output Frequency	-	24.5760	-	MHz
Frequency Tolerance		+/- 10		ppm
Output Duty Cycle	48	-	52	%
RMS Phase Jitter (Random)	-	0.5	-	ps
Main Clock Output Impedance	-	50	-	Ohm
Aux1 Clock Output Impedance	-	7	-	Ohm
Aux2 Clock Output Impedance	-	7	-	Ohm

Table 3: Performance specifications.

2.5 Pin Descriptions

PIN #	Name	I/O	Description
1	DGND1	Ground	Ground for I/O and core logic.
2	NC	Input	Cut Pin
3	DGND3	Ground	Ground for I/O and core logic.
4	NC	Input	Not used – Connect to GND.
5	DGND5	Ground	Ground for I/O and core logic.
6	VCC	Power	Digital Power - Digital core power supply +5V.
7	DGND7	Ground	Ground for I/O and core logic.
8	NC	Input	Not used – Connect to GND.
9	DGND9	Ground	Ground for I/O and core logic.
10	NC	Input	Not used – Connect to GND.
11	DGND11	Ground	Ground for I/O and core logic.
12	NC	Input	Not used – Connect to GND.
13	DGND13	Ground	Ground for I/O and core logic.
14	$\overline{\text{ENABLE}}$	Input	Clock Enable – enables / disables clocks.
15	DGND15	Ground	Ground for I/O and core logic.
16	DGND16	Ground	Ground for I/O and core logic.

17	DGND17	Ground	Ground for I/O and core logic.
18	DGND18	Ground	Ground for I/O and core logic.
19	NC	Input	Not used – Connect to GND.
20	DGND20	Ground	Ground for I/O and core logic.
21	NC	Input	Not used – Connect to GND.
22	DGND22	Ground	Ground for I/O and core logic.
23	MAIN_OUT	Output	Main Clock for directly driving 50ohm loads
24	DGND24	Ground	Ground for I/O and core logic.
25	AUX1_OUT	Output	AUX Clock with no impedance adaptation
26	DGND26	Ground	Ground for I/O and core logic.
27	AUX2_OUT	Output	AUX Clock with no impedance adaptation
28	DGND28	Ground	Ground for I/O and core logic.
29	NC	Input	Not used – Connect to GND.
30	DGND30	Ground	Ground for I/O and core logic.
31	NC	Input	Not used – Connect to GND.
32	DGND32	Ground	Ground for I/O and core logic.

Table 4: Pinout description.

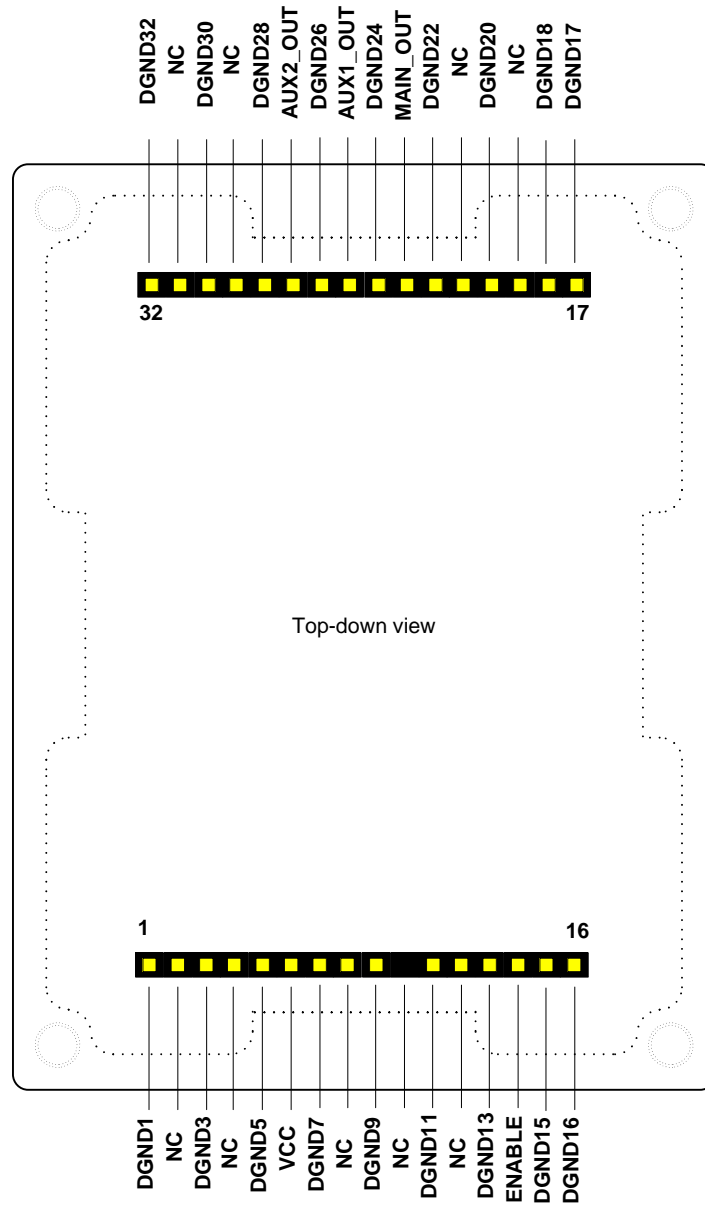


Figure 4: Pinout – top down view.

3 Interfacing and Operation

This chapter provides practical application information for hardware and systems engineers who will be designing the TimeLock™ Module into their product.

3.1 General Description

The TimeLock™ Module allows audio system designers to incorporate a high quality, ultra-low jitter master clock source for driving audio critical ICs, such as S/PDIF receivers, transmitter, DACs, ADCs, Audio Processors etc.. in sensitive and demanding audio conversion applications. The master clock provides a very stable and low jitter clock source that is typically used in combination with sample rate converters or upsamplers, such as the Quantum™ and Sonic2™ digital audio processing modules from ANAGRAM Technologies.

3.2 Typical Connections

The TimeLock™ Module is operated in hardware mode with only one control input line (clock signal enable).

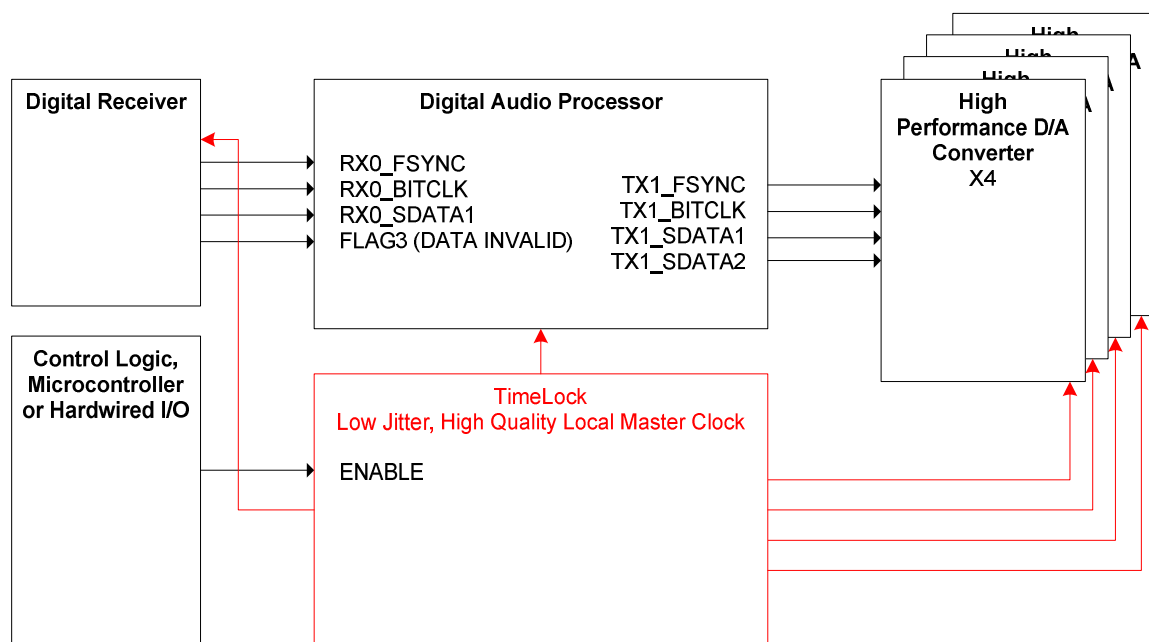


Figure 5: Typical connection diagram.

3.3 Interfacing to High Performance D/A Converters

The TimeLock Module is designed specifically to clock high performance D/A converter subsystems. Connection to the Sonic2 and TimeLock Module with dual DACs is given in Figure 6.

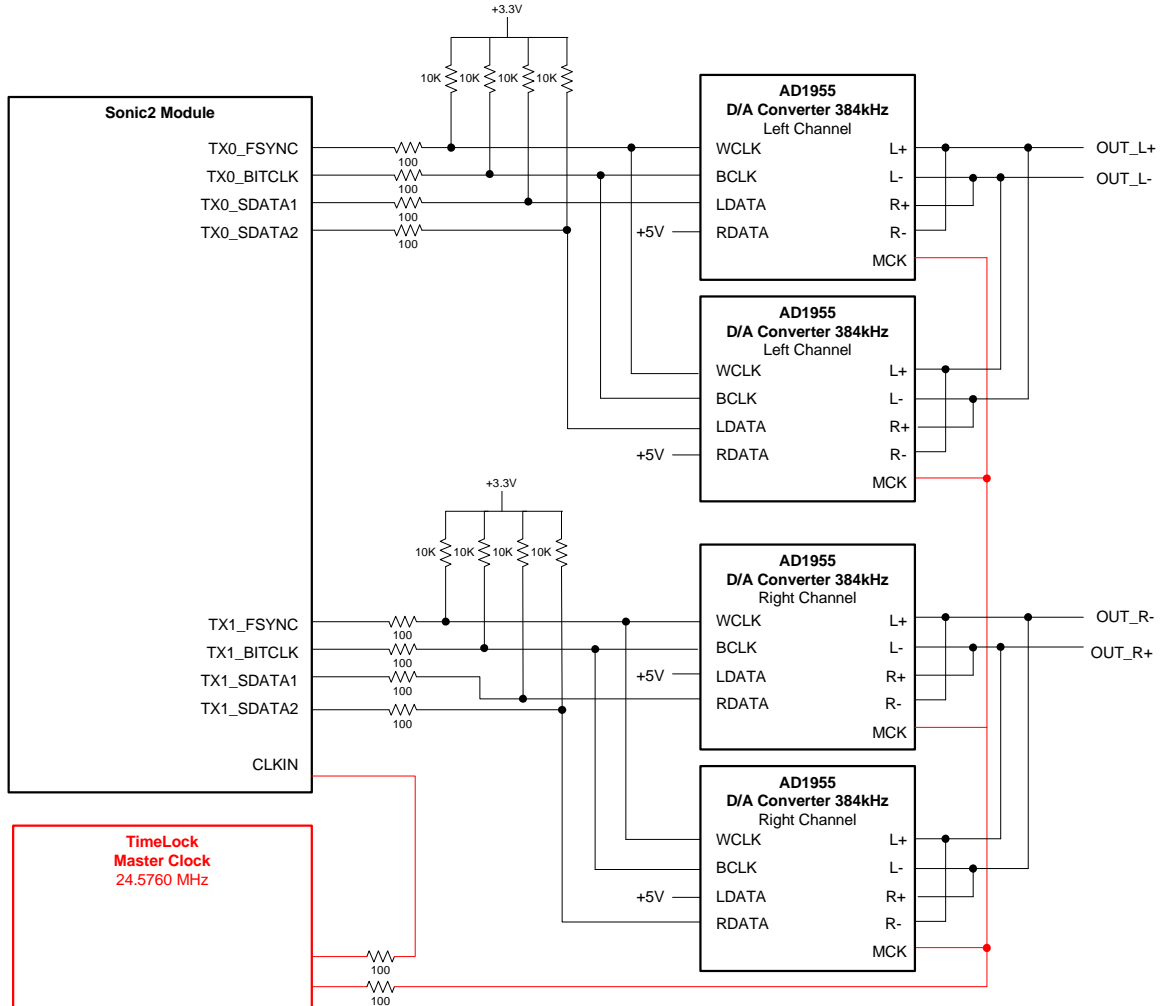


Figure 6: Interfacing with digital audio processing and high performance D/A converters.

3.4 Clock Enable

The TimeLock™ Module clock outputs may be synchronously enabled or disabled by the ENABLE, active low signal. A minimum of 4 clock cycles must be waited before the output clocks are disabled.

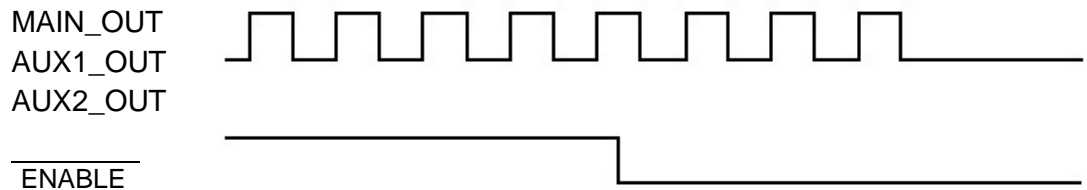


Table 5: Clock enable timing requirements.

3.5 Clock Terminations

To handle high speed LVCMOS drivers, general rules for high-speed digital board design must be carefully followed. Improper handling of the termination will cause signal reflection, clock ringing and lead to system failure. Proper termination is required to ensure signal integrity and Electro-Magnetic Interference (EMI) reduction. There are many different termination schemes for single ended LVCMOS drivers. This section discusses parallel termination, AC termination and series termination. The following termination approaches are only general recommendations under ideal conditions. Board designers should consult with their signal integrity engineers and verify through simulations in their system environment.

3.5.1 Parallel Termination

The standard termination of an LVCMOS driver in a $Z_o=50\Omega$ transmission line environment is shown in Figure 7. The driver is terminated with 50 Ohm pull down to 1.7V at the receiver end. In actual applications, the equivalent parallel termination shown in Figure 8 can be used. The LVCMOS parallel termination has the same effect as the standard LVCMOS shown in Figure 7. The parallel termination shown in Figure 8 can eliminate the need of split power supply (or reference voltage). The power dissipation calculation is beyond the scope of this document.

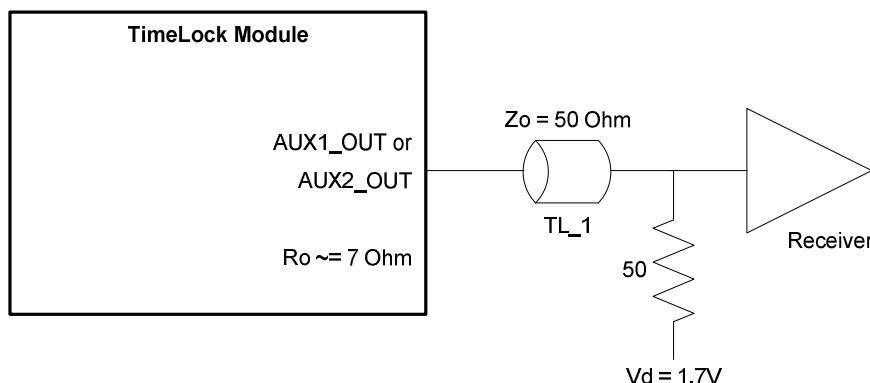


Figure 7: Parallel clock termination pull down.

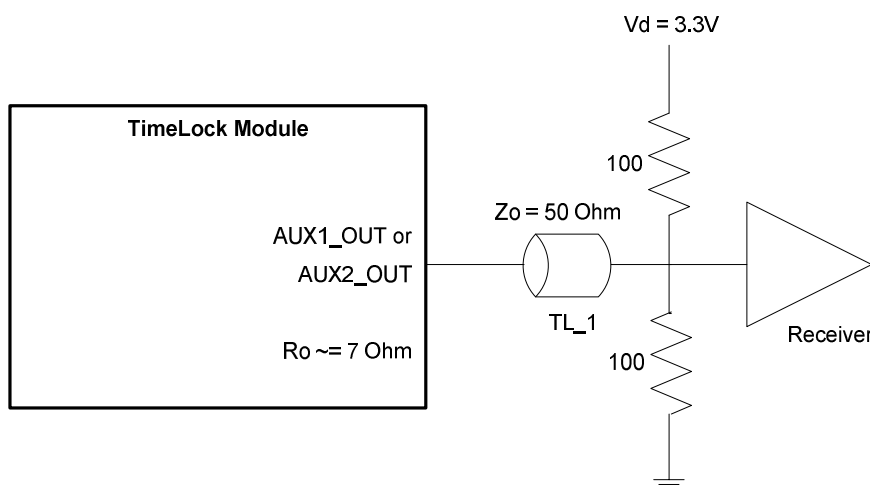



Figure 8: Parallel clock termination split pull-up/down.

Note	
	<p><i>If parallel termination is required it is recommended to use AUX1 or AUX2 clock outputs of the TimeLock™ Module that have a lower impedance than the MAIN clock output.</i></p>

3.5.2 AC Termination

The LVCMOS driver AC termination in a 50Ω transmission line environment is shown in Figure 9. The majority of load current is drawn during transient region (i.e. rising edge and falling edge). This termination consumes less power than the parallel termination. The proper value of capacitor C1 depends on the trace delay and capacitance of the transmission line.

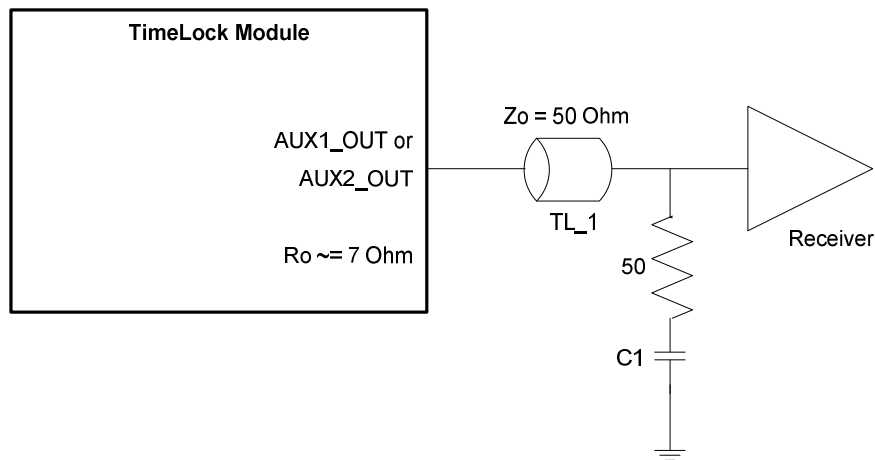



Figure 9: AC clock termination.

Note	
	<p><i>If AC termination is required it is recommended to use AUX1 or AUX2 clock outputs of the TimeLock™ Module that have a lower impedance than the MAIN clock output.</i></p>

3.5.3 Series Termination

Series termination is a popular termination scheme for LVCMOS drivers. Figure 10 shows a simple series termination for LVCMOS drivers with the Main and Auxiliary clock outputs. The main differences between the main and auxiliary clock outputs is the output impedance of 50Ω and 7Ω respectively.

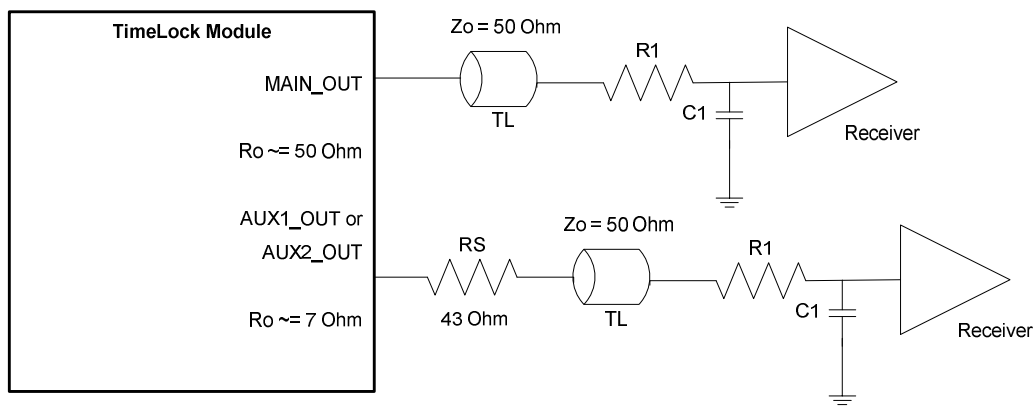


Figure 10: One to one LVCMOS termination.

The typical output impedance R_o of the TimeLock™ Module LVCMOS driver is approximately 7 ohms for AUX1 and AUX2. It is 50Ω for the MAIN clock output. (Some parts might have slightly different R_o values. The closest series resistor value, R_s , can be calculated as follows

$$R_s = Z_o - R_o = 43\Omega$$

In the Figure 10, the footprint for optional series resistor R1 or optional capacitor C1 at the receiver input is recommend for adjusting edge rate or overshoot if necessary.

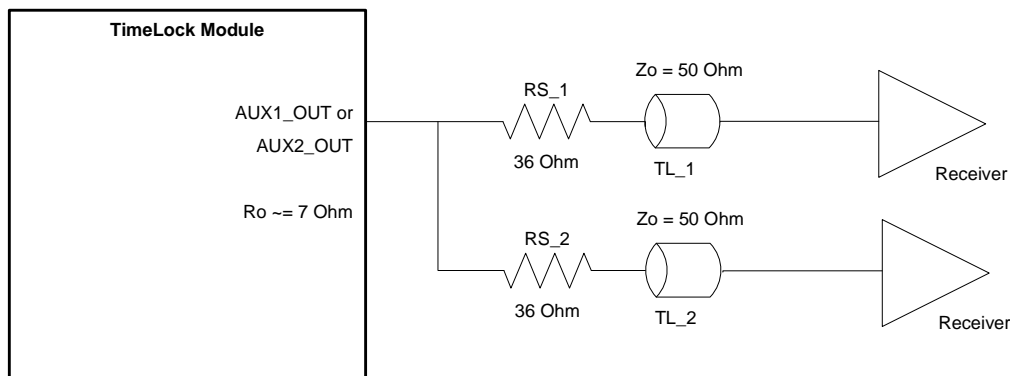


Figure 11: Series termination of one LVCMOS driver driving two receivers.

Another common configuration of series termination is one driver driving 2 receivers as shown in Figure 11, with $N=1$ and $M=2$, the series resistor is calculated to be $R_s = 36\Omega$. The trace delays on TL_1 and TL_2 are assumed to be equal as should the loading conditions on both receivers. When the number of drivers is not equal to number of receivers as shown in Figure 12, the series resistor value R_s is calculated as follows:

$$R_s = Z_o - (R_o \times M) / (N)$$

Number of driver = N
 Number of receiver = M

This configuration assumes that all the trace delays and load conditions are equally matched.

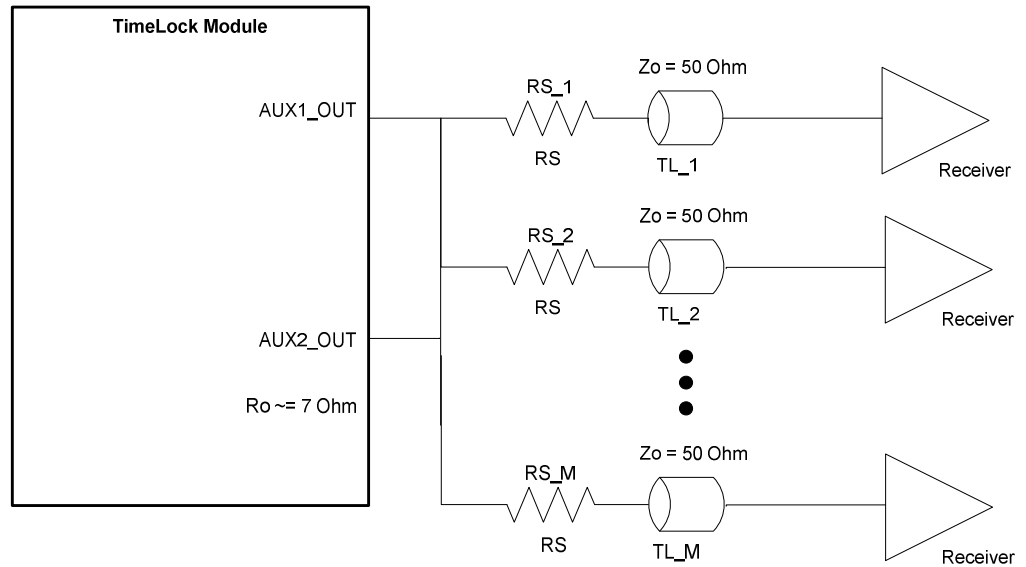


Figure 12: Two LVC MOS drivers tied together to driver M receivers.

For 2 drivers driving 6 receivers, the closest series resistor can be calculated as follows:

$$N=2, N=6, Z_o=50\Omega, R_o=7\Omega$$

$$R_s = 50 - (7 \times 6)/2 = 29\Omega$$

The result above is straight from calculations. The closest available resistor value should be chosen.

4 Packaging and Dimensions

This chapter provides the physical packaging dimensions for the TimeLock™ Module.

4.1 Package Dimensions Metric

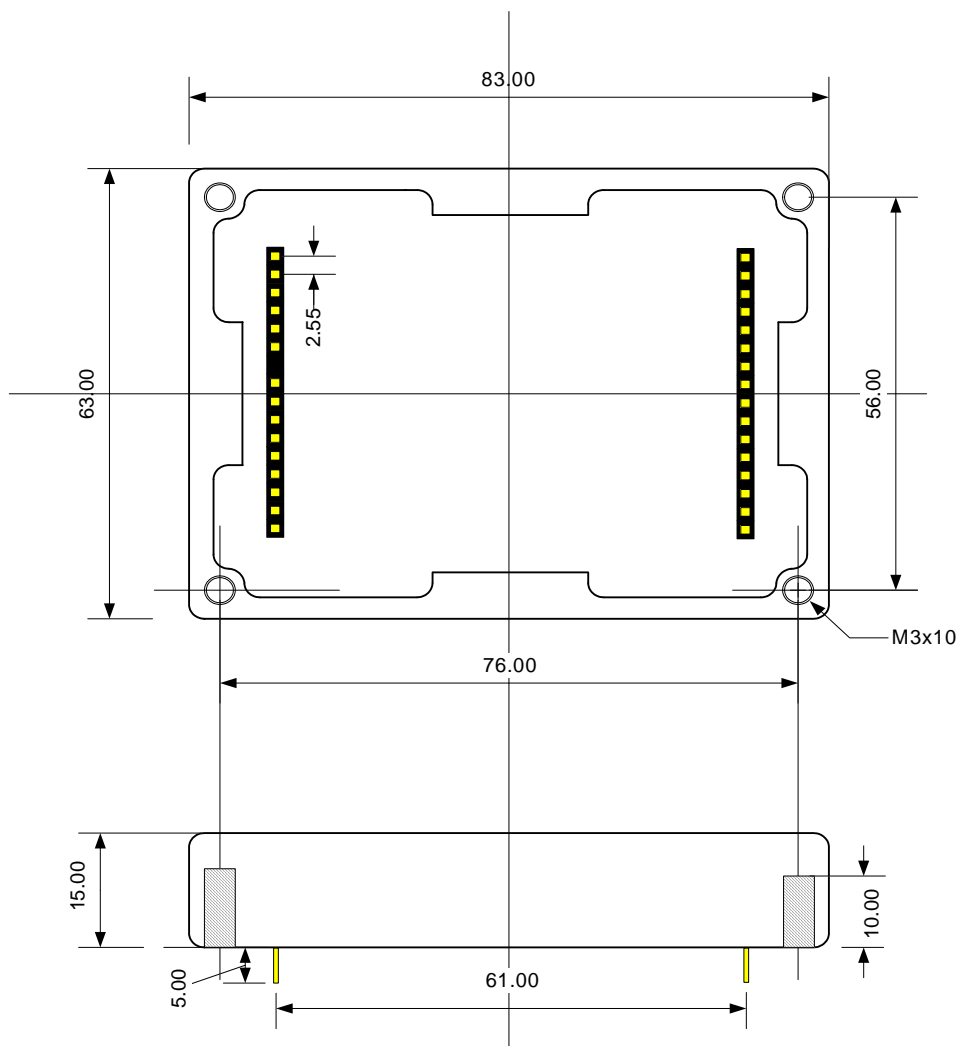


Figure 13: Module housing – physical dimensions (metric).